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EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/060,454	MUROOR, SRIKANTH R.
	Examiner	Art Unit
	Thomas J. Cleary	2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 9-12, and 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") and US Patent Number 3,886,543 to Marin ("Marin").

3. In reference to Claim 1, AAPA teaches a bus arbitrator comprising: an input circuit receiving a first bus access request signal from a first bus device (See Figure 2 'REQ1') and a second bus access request signal from a second bus device (See Figure 2 'REQ2'), the input circuit outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Numbers 215 and 220). The AND gate and inverter of the input circuit inherently have a first delay. Because REQ1 does not pass through the AND gate and inverter of the input circuit in generating EN1, the first delay does not delay high-to-low transitions in

the first line driver enable signal (See Figure 2). AAPA does not teach a delay circuit generating a time-delayed first bus access request signal from the first bus access request signal, and a time-delayed second bus access request signal from the second bus access request signal, the delay circuit associated with a second delay; and a comparator circuit generating a first line driver enable signal only if both the first bus access request signal and the time-delayed first bus access request signal are enabled, and generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the first and second line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay. Marin teaches a delay circuit which receives a signal (See Figures 2 and 3 Letter A) and generates a time-delayed version of the signal (See Figures 2 and 3 Letter B), and a comparator circuit which generates an output signal only if both of the signal and the time-delayed signal are enabled (See Figure 2 Number 62 and Column 7 Lines 50-59). The delay circuit delays low-to-high transitions of the output signal by less than one-half of the clock cycle of the clock signal (See Figure 3 Letters A and B and 'STEP'). Because the first delay of AAPA is simply the propagation delay of a chain of two basic gates, the first delay is shorter than that provided by the delay circuit of Marin, which is equal to the time for shifting the input through a shift register.

It would have been obvious to one or ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay and comparator circuits of Marin on both the first enable signal (See Figure 2 'EN1' of AAPA) and the second enable signal (See Figure 2 'EN2' of AAPA), resulting in the invention of Claim 1, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

4. In reference to Claim 2, AAPA and Marin teach the limitations as applied to Claim 1 above. Marin further teaches using an AND gate as the comparator circuit for comparing the signal and the delayed signal, and thus the output of the AND gate will inherently be disabled if either the signal or the delayed signal is disabled, since the output of an AND gate is only enabled when all of its inputs are enabled (See Figure 2 Number 62 and Column 7 Lines 50-59).

5. In reference to Claim 3, AAPA and Marin teach the limitations as applied to Claim 2 above. Marin further teaches that the time delay of the delay circuit is equal to the time for shifting the input through a shift register, which is inherently much greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate (See Figure 2 Number 50 and Column 7 Lines 46-50).

6. In reference to Claim 4, AAPA and Marin teach the limitations as applied to Claim 3 above. Marin further teaches that said comparator circuit comprises an AND gate having a first input for receiving a the signal and a second input for receiving the time-delayed signal (See Figure 2 Number 62 and Column 7 Lines 56-61).

7. In reference to Claim 9, AAPA teaches a shared bus system comprising: N bus devices (See Figure 2 'REQ1' and 'REQ2') capable of requesting access to a shared bus (See Figure 2 Number 240); M tristate line drivers (See Figure 2 Number 230A and 230B), each of said the M tristate line drivers having an input for receiving a logic bit from one of said the N bus devices and an output for outputting said the received logic bit to said the shared bus (See Figure 2 'DB1'), wherein said each tristate line driver outputs said the received logic bit when a line driver enable signal associated with the respective tristate line driver is enabled and an output of said each tristate line driver is put into a high-impedance state when said the associated line driver enable signal is disabled (See Figure 3); a bus arbitrator operable to activate and de-activate the M tristate line drivers (See Figure 2 Number 210), the bus arbitrator comprising: an input circuit capable of receiving a first bus access request signal from a first of the N bus devices (See Figure 2 'REQ1') and a second bus access request signal from a second of the N bus devices (See Figure 2 'REQ2'), the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Numbers 215 and 220). The AND gate and

inverter of the input circuit inherently have a first delay. Because REQ1 does not pass through the AND gate and inverter of the input circuit in generating EN1, the first delay does not delay high-to-low transitions in the first line driver enable signal (See Figure 2). AAPA does not teach a delay circuit capable of receiving the first bus access request signal and generating therefrom a time-delayed first bus access request signal, the delay circuit also capable of receiving the second bus access request signal and generating therefrom a time-delayed second bus access request signal, the delay circuit associated with a second delay; and a comparator circuit capable of generating a first line driver enable signal only if both the first bus access request signal and said the time-delayed first bus access request signal are enabled, the comparator circuit also capable of generating a second line driver enable signal only if both the second bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay. Marin teaches a delay circuit which receives a signal (See Figures 2 and 3 Letter A) and generates a time-delayed version of the signal (See Figures 2 and 3 Letter B), and a comparator circuit which generates an output signal only if both of the signal and the time-delayed signal are enabled (See Figure 2 Number 62 and Column 7 Lines 50-59). The delay circuit delays low-to-high transitions of the output signal by less than one-half of the clock cycle of the clock signal (See Figure 3 Letters A and B and 'STEP'). Because the first delay of AAPA is simply

the propagation delay of a chain of two basic gates, the first delay is shorter than that provided by the delay circuit of Marin, which is equal to the time for shifting the input through a shift register.

It would have been obvious to one or ordinary skill in the art at the time the invention was made to construct the device of AAPA with the delay and comparator circuits of Marin on both the first enable signal (See Figure 2 'EN1' of AAPA) and the second enable signal (See Figure 2 'EN2' of AAPA), resulting in the invention of Claim 9, in order to provide a debounce delay period which ensures that the signal has reached a steady state and thus increases the fault tolerance (See Column 7 Lines 50-52 of Marin).

8. Claim 17 recites limitations which are substantially equivalent to those of Claim 9 and is rejected under similar reasoning as applied to Claim 9 above.

9. In reference to Claim 10, AAPA and Marin teach the limitations as applied to Claim 9 above. Marin further teaches using an AND gate as the comparator circuit for comparing the signal and the delayed signal, and thus the output of the AND gate will inherently be disabled if either the signal or the delayed signal is disabled, since the output of an AND gate is only enabled when all of its inputs are enabled (See Figure 2 Number 62 and Column 7 Lines 50-59).

10. Claim 18 recites limitations which are substantially equivalent to those of Claim 10 and is rejected under similar reasoning as applied to Claim 10 above.

11. In reference to Claim 11, AAPA and Marin teach the limitations as applied to Claim 10 above. Marin further teaches that the time delay of the delay circuit is equal to the time for shifting the input through a shift register, which is inherently much greater than the maximum de-activation delay period, which is equivalent to the switching time of the AND gate (See Figure 2 Number 50 and Column 7 Lines 46-50).

12. Claim 19 recites limitations which are substantially equivalent to those of Claim 11 and is rejected under similar reasoning as applied to Claim 11 above.

13. In reference to Claim 12, AAPA and Marin teach the limitations as applied to Claim 11 above. Marin further teaches that said comparator circuit comprises an AND gate having a first input for receiving a the signal and a second input for receiving the time-delayed signal (See Figure 2 Number 62 and Column 7 Lines 56-61).

14. Claim 20 recites limitations which are substantially equivalent to those of Claim 12 and is rejected under similar reasoning as applied to Claim 12 above.

15. In reference to Claim 21, AAPA and Marin teach the limitations as applied to Claim 1 above. AAPA further teaches an inverter capable of receiving and inverting the

first bus access request signal (See Figure 2 Number 215); and an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal (See Figure 2 Number 220), the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled (See Figure 2 Number 210).

16. Claims 5, 6, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Marin as applied to Claims 3 and 9 above, and further in view of US Patent Number 5,306,963 to Leak et al. ("Leak").

17. In reference to Claims 5 and 6, AAPA and Marin teach the limitations as applied to Claim 3 above. AAPA and Marin do not teach that the delay circuit is an asynchronous delay circuit comprising a first set of an even number of inverters connected in series, wherein a first inverter in the first set receives the first bus access request signal and a last inverter in the first set generates the time-delayed first bus access request signal; and a second set of an even number of inverters connected in series, wherein a first inverter in the second set receives the second bus access request signal and a last inverter in the second set generates the time-delayed second bus access request signal. Leak teaches an asynchronous delay chain comprising an even number of inverters wherein the first inverter in the chain receives a signal at its input

and the last inverter in the chain generates a time-delayed version of the input signal (See Figure 1 and Column 4 Lines 3-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Marin using the delay chain of Leak, resulting in the inventions of Claims 5 and 6, because a delay chain is simpler to construct than a flip-flop; a delay chain does not require a clock signal; and the switching time of an inverter in a delay chain is faster than the clock signal used by a flip-flop, thus providing a higher resolution when setting the delay time. Further, the delay chain of Leak is used for an equivalent purpose as the shift register delay circuit of Marin, namely providing a signal to one input of a comparison circuit and providing a delayed version of said signal to the other input of said comparison circuit (See Figure 1 and Column 4 Lines 3-55 of Leak; and Figure 2 and Column 7 Lines 46-50 of Marin).

18. In reference to Claims 13 and 14, AAPA and Marin teach the limitations as applied to Claim 11 above. AAPA and Marin do not teach that the delay circuit is an asynchronous delay circuit comprising a first set of an even number of inverters connected in series, wherein a first inverter in the first set receives the first bus access request signal and a last inverter in the first set generates the time-delayed first bus access request signal; and a second set of an even number of inverters connected in series, wherein a first inverter in the second set receives the second bus access request signal and a last inverter in the second set generates the time-delayed second bus access request signal. Leak teaches an asynchronous delay chain comprising an even

number of inverters wherein the first inverter in the chain receives a signal at its input and the last inverter in the chain generates a time-delayed version of the input signal (See Figure 1 and Column 4 Lines 3-37).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Marin using the delay chain of Leak, resulting in the inventions of Claims 13 and 14, because a delay chain is simpler to construct than a flip-flop; a delay chain does not require a clock signal; and the switching time of an inverter in a delay chain is faster than the clock signal used by a flip-flop, thus providing a higher resolution when setting the delay time. Further, the delay chain of Leak is used for an equivalent purpose as the shift register delay circuit of Marin, namely providing a signal to one input of a comparison circuit and providing a delayed version of said signal to the other input of said comparison circuit (See Figure 1 and Column 4 Lines 3-55 of Leak; and Figure 2 and Column 7 Lines 46-50 of Marin).

19. Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Marin as applied to Claims 3 and 11 above, and further in view of Computer Aided Logical Design With Emphasis on VLSI, Fourth Edition, by Frederick J. Hill et al. ("Hill").

20. In reference to Claims 7 and 8, AAPA and Marin teach the limitations as applied to Claim 3 above. Marin further teaches that the delay circuit is a synchronous delay circuit (See Figure 2 Number 50) having a flip flop (See Figure 2 Number 50) having an

input receiving a first signal (See Figure 2 Letter A) and an output (See Figure 2 Letter B) coupled to a comparator circuit that generates the time delayed first signal (See Figure 2 Number 62). Marin does not explicitly teach an inverter having an input receiving the clock signal and an output coupled to a clock input of the flip flop. However, Marin does teach that the clock signal is connected to the clock input of the flip flop through an AND gate (See Figure 2 Number 60). Hill teaches that in CMOS technology, an AND gate is formed by connecting the output of a NAND gate to an inverter (See Figures 4.3, 4.4, and 4.6 and Page 55 Paragraph 3). Thus, when constructed in CMOS technology, the AND gate of Marin is inherently constructed of a NAND gate and an inverter, and the clock signal passing through the AND gate inherently passes through an inverter having an output coupled to a clock input of the first flip flop.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Marin using CMOS technology, resulting in the invention of Claims 7 and 8, because CMOS technology is the most widely used VLSI technology (See Page 54 Section 4.1 of Hill).

21. In reference to Claims 15 and 16, AAPA and Marin teach the limitations as applied to Claim 11 above. Marin further teaches that the delay circuit is a synchronous delay circuit (See Figure 2 Number 50) having a flip flop (See Figure 2 Number 50) having an input receiving a first signal (See Figure 2 Letter A) and an output (See Figure 2 Letter B) coupled to a comparator circuit that generates the time delayed first

signal (See Figure 2 Number 62). Marin does not explicitly teach an inverter having an input receiving the clock signal and an output coupled to a clock input of the flip flop. However, Marin does teach that the clock signal is connected to the clock input of the flip flop through an AND gate (See Figure 2 Number 60). Hill teaches that in CMOS technology, an AND gate is formed by connecting the output of a NAND gate to an inverter (See Figures 4.3, 4.4, and 4.6 and Page 55 Paragraph 3). Thus, when constructed in CMOS technology, the AND gate of Marin is inherently constructed of a NAND gate and an inverter, and the clock signal passing through the AND gate inherently passes through an inverter having an output coupled to a clock input of the first flip flop.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Marin using CMOS technology, resulting in the invention of Claims 15 and 16, because CMOS technology is the most widely used VLSI technology (See Page 54 Section 4.1 of Hill).

Response to Arguments

22. Applicant's arguments filed 31 October 2005 have been fully considered but they are not persuasive. Applicant has argued that the high-to-low transitions in the second line driver enable signal are delayed differently than high-to-low transitions in the first line driver enable signal. In response, the Examiner notes that because elements 215 and 220 of AAPA provide a delay on the second line driver enable signal but not on the

first line driver enable signal, all transitions, including high-to-low transitions, have a longer delay for the second line driver enable signal than for the first line driver enable signal. It is unclear what Applicant is referring to with the statement "by not introducing the second delay to the first line driver enable signal". Applicant's Figure 4 clearly shows that the delay circuit which provides the second delay (Number 420) is present on both the first and second line driver enable signals. Further, it is noted that Claims 1, 9, and 17 each recite that "the first delay...does not delay high-to-low transitions in the first line driver enable signal". The features upon which applicant relies (i.e., not introducing the second delay to the first line driver enable signal) are not recited in the rejected claim(s).

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

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